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UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7003023 B2  
APPLICATION NO. : 10/672,259  
ISSUE DATE : 02-21-06  
INVENTOR(S) : Krone et. al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby  
corrected as shown below

THE TILTE PAGE, SHOWING AN ILLUSTRATIVE FIGURE, SHOULD BE **DELETED** AND **SUBSTITUTE** THEREFOR THE ATTACHED TITLE PAGE.

**DELETE** DRAWING SHEETS 1-15, AND **SUBSTITUTE** THEREFOR THE DRWAING SHEETS CONSISTING OF FIGS 1-15 AS SHOWN ON THE ATTACHED PAGES.

column 26, line 64, delete "baffler" and insert --barrier--.  
column 26, line 65, delete "baffler" and insert --barrier--.  
column 27, line 6, delete "baffler" and insert --barrier--.  
column 27, line 9, delete "baffler" and insert --barrier--.  
column 27, line 12, delete "baffler" and insert --barrier--.  
column 27, line 13, delete "baffler" and insert --barrier--.  
column 27, line 15, delete "baffler" and insert --barrier--.  
column 27, line 17, delete "baffler" and insert --barrier--.  
column 27, line 18, delete "baffler" and insert --barrier--.  
column 27, line 21, delete "baffler" and insert --barrier--.  
column 27, line 23, delete "baffler" and insert --barrier--.  
column 27, line 26, delete "baffler" and insert --barrier--.  
column 28, line 1, delete "baffler" and insert --barrier--.  
column 28, line 3, delete "baffler" and insert --barrier--.



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(12) **United States Patent**  
**Krone et al.**

(10) Patent No.: **US 7,003,023 B2**(45) Date of Patent: **\*Feb. 21, 2006**

(54) **DIGITAL ISOLATION SYSTEM WITH ADC  
OFFSET CALIBRATION**

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(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 278 days.

This patent is subject to a terminal dis-  
claimer.

(21) Appl. No.: **10/672,259**

(22) Filed: **Sep. 26, 2003**

(65) **Prior Publication Data**

**US 2004/0057524 A1 Mar. 25, 2004**

**Related U.S. Application Data**

(60) Continuation of application No. 10/161,902, filed on  
Jun. 4, 2002, which is a division of application No.  
09/035,180, filed on Mar. 4, 1998, now Pat. No.  
6,442,213, which is a continuation-in-part of appli-  
cation No. 08/841,409, filed on Apr. 22, 1997, now  
Pat. No. 6,137,827, and a continuation-in-part of  
application No. 08/837,702, filed on Apr. 22, 1997,  
now Pat. No. 5,870,046, and a continuation-in-part of  
application No. 08/837,714, filed on Apr. 22, 1997,  
now Pat. No. 6,430,229.

(51) Int. Cl.  
**H04B 1/38 (2006.01)**

(52) U.S. Cl. .... 375/219; 341/143

(58) Field of Classification Search ..... 375/219-222,  
375/259; 341/143  
See application file for complete search history.

(56) **References Cited**  
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LLP

(57) **ABSTRACT**

An improved digital capacitive isolation barrier system is  
provided that is suitable for use in a telephone or modem  
where the locally powered circuits must be effectively  
isolated from the public telephone system, while permitting  
data transfer across the barrier. In particular, an automatic  
ADC offset calibration system is provided for determining  
the magnitude of the ADC offset signal required in the  
system during a calibration operation, and for providing the  
calibrated ADC offset signal during normal operation of the  
isolation barrier system. A modified hybrid circuit is pro-  
vided for isolating the system input from the telephone line  
during calibration, and for completing the calibration loop.  
Fixed bias signals are also provided for the ADC and for a  
DAC in the system. In a preferred embodiment, the ADC is  
located on the isolated side of the isolation barrier, while the  
integrator and register that determine and hold the offset  
signal are located on the powered side of the isolation  
barrier.

16 Claims, 15 Drawing Sheets

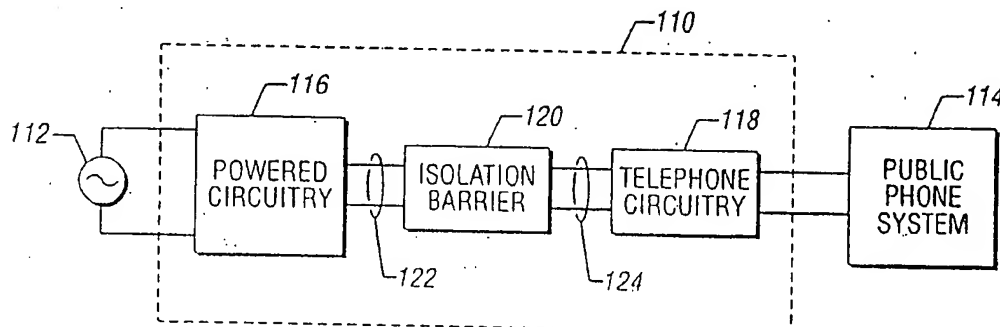


FIG. 1

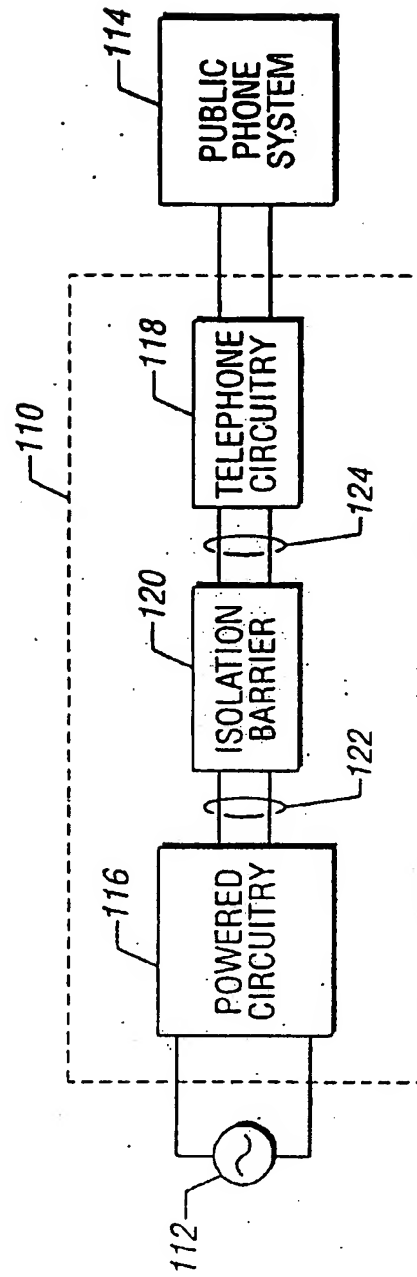
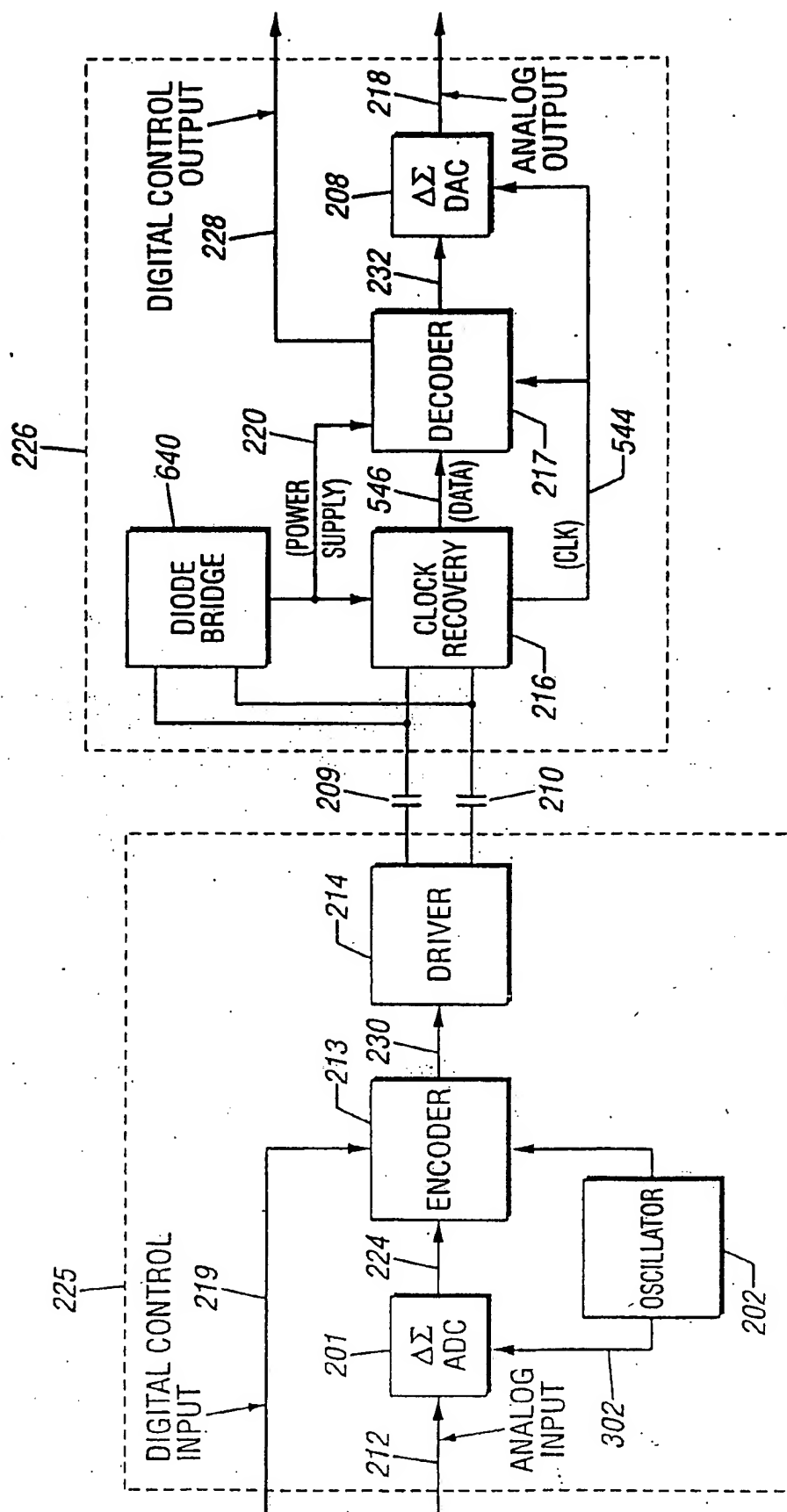
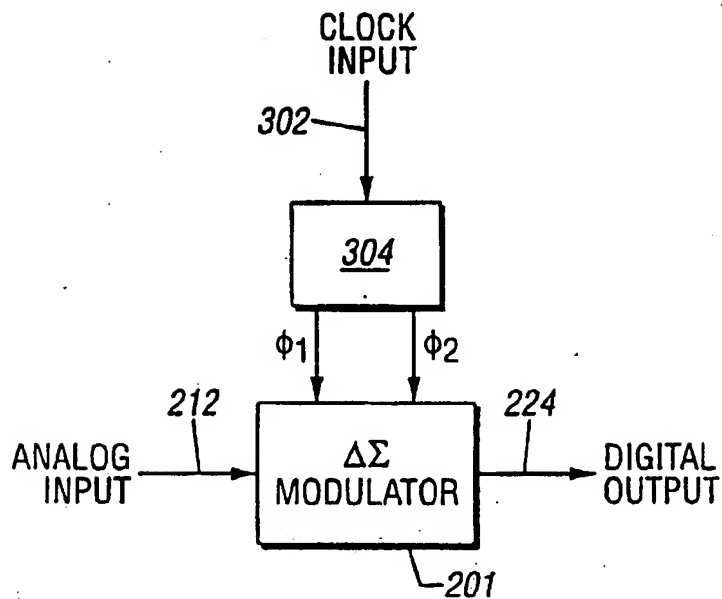


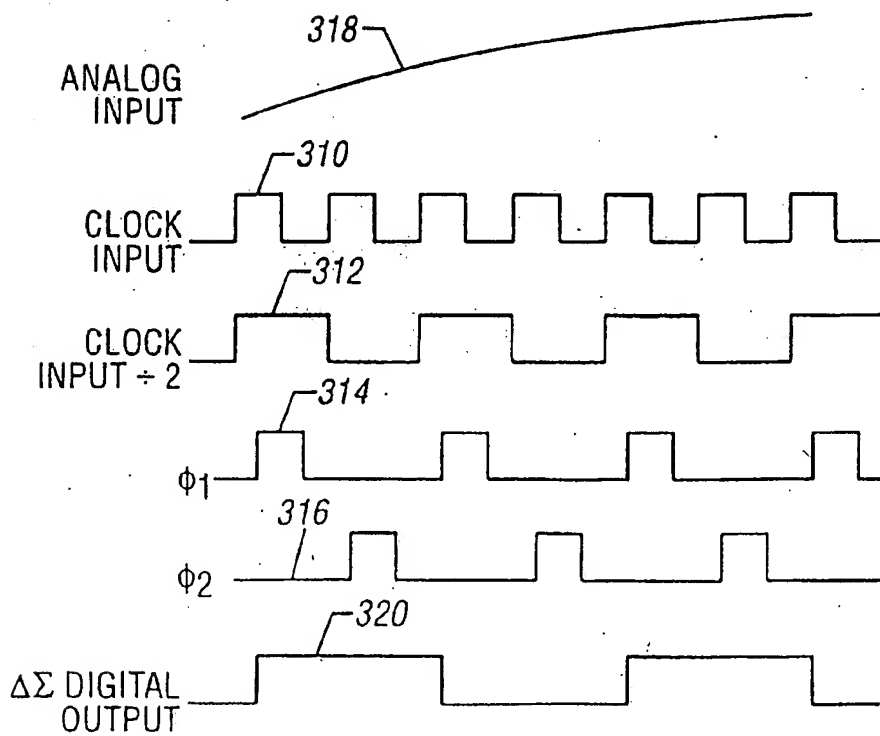
FIG. 2



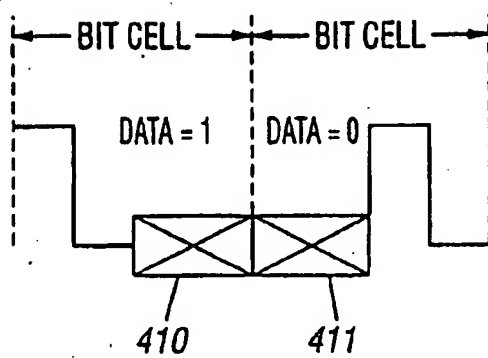
**FIG. 3A**



**FIG. 3B**



**FIG. 4A**



**FIG. 4B**

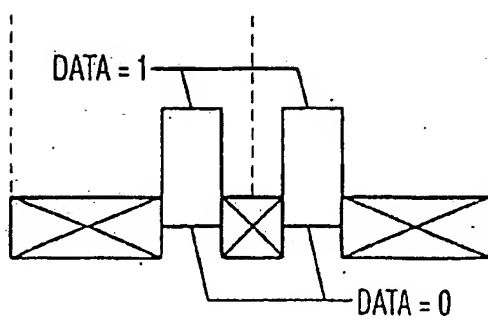
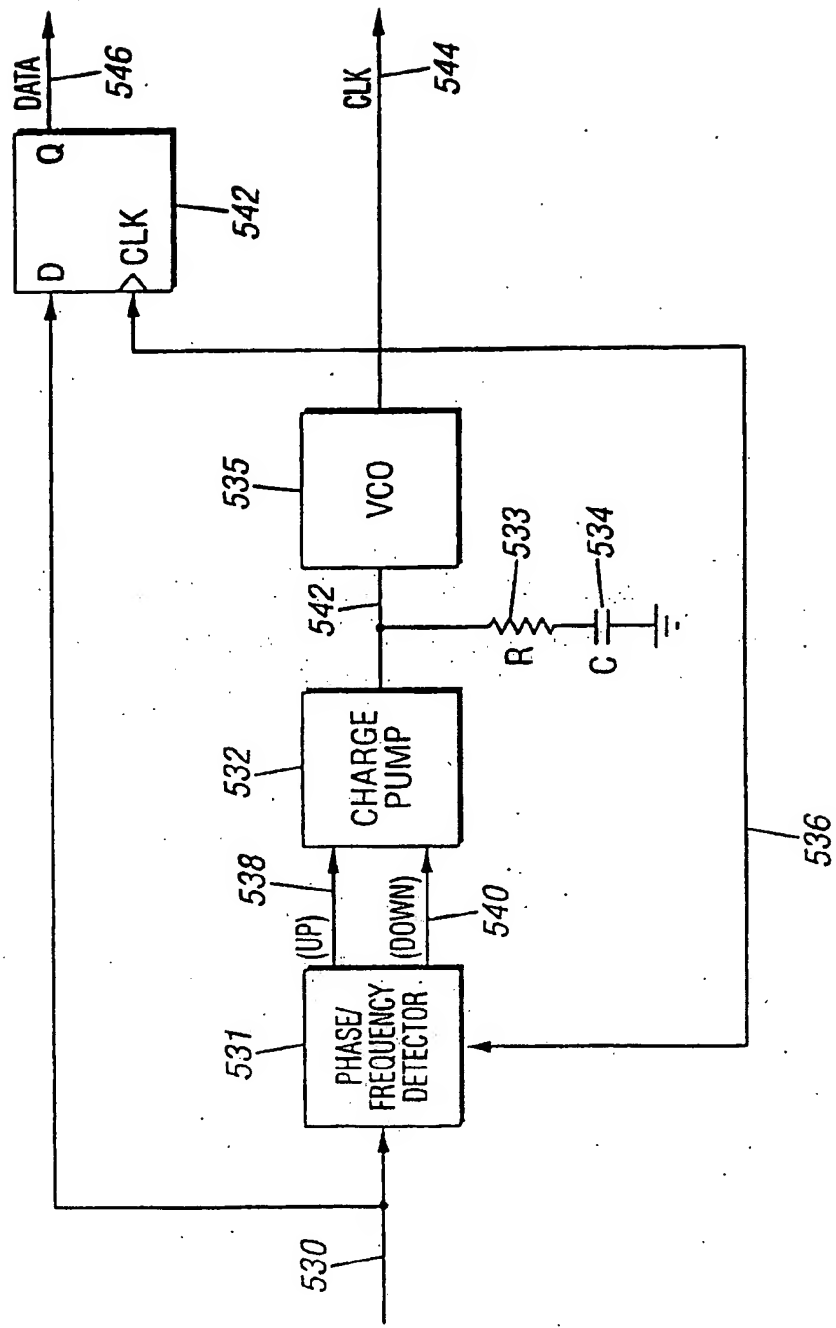
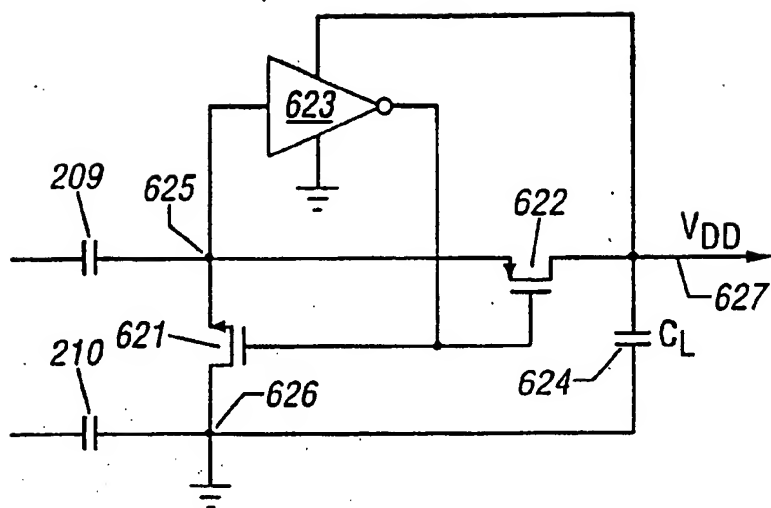


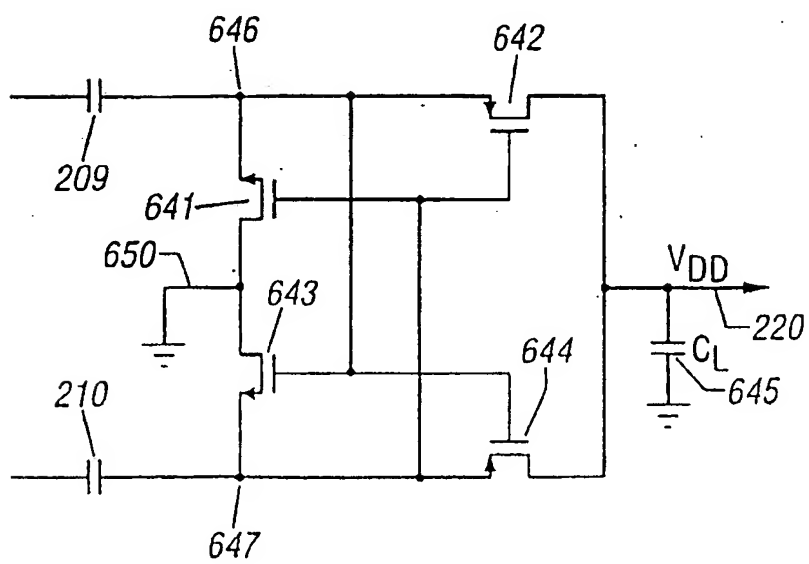
FIG. 5



**FIG. 6A**



**FIG. 6B**





**FIG. 7**

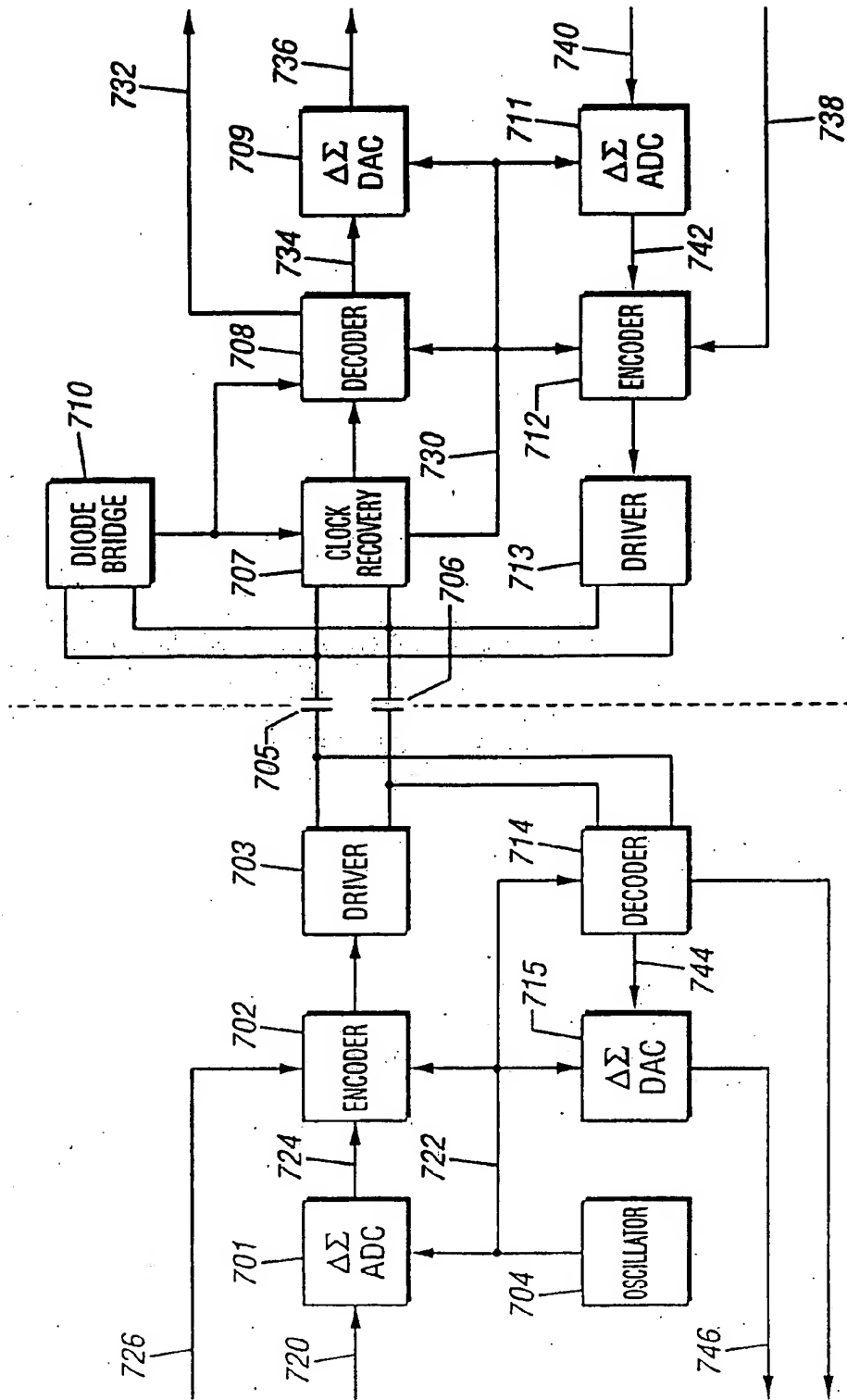


FIG. 8

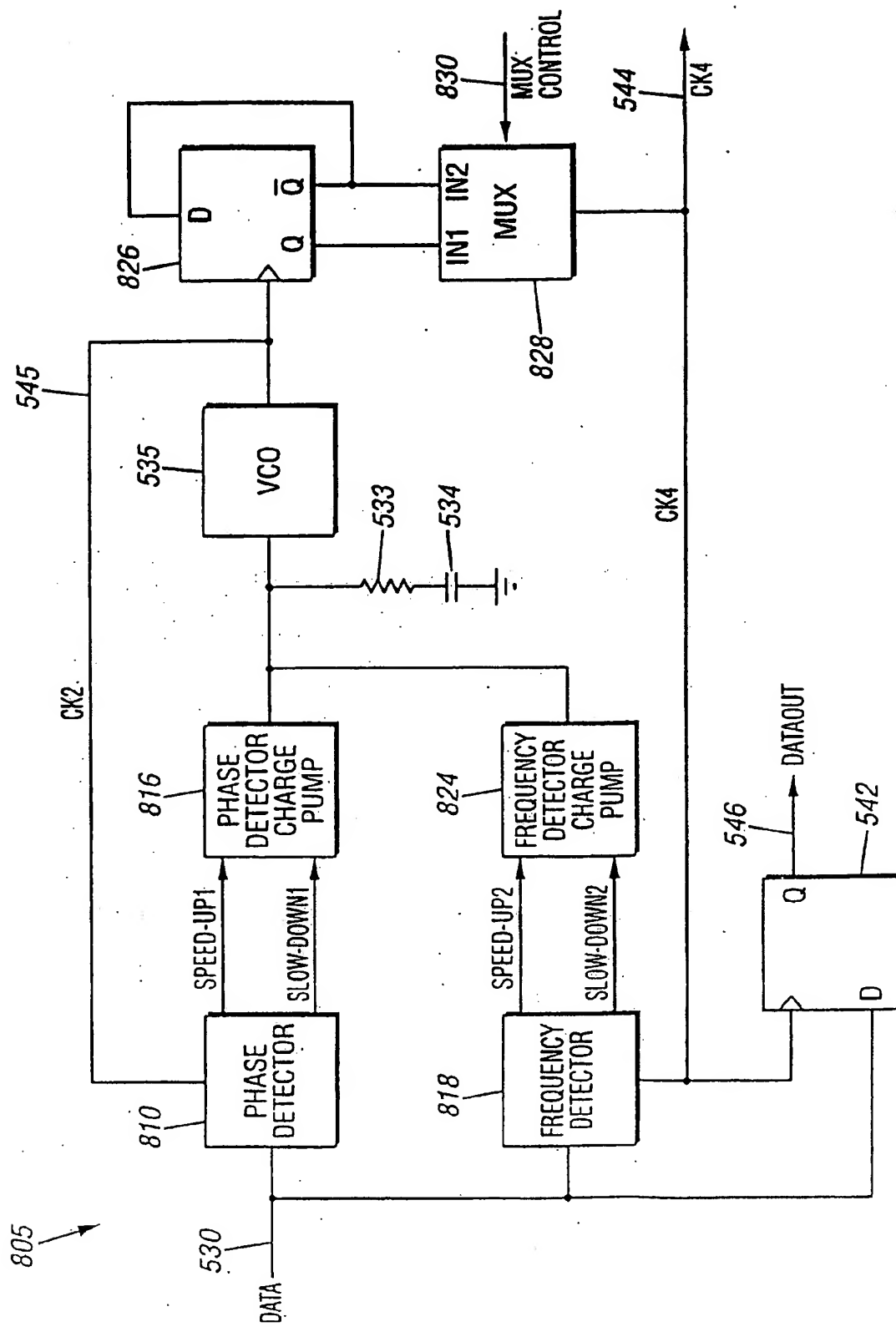
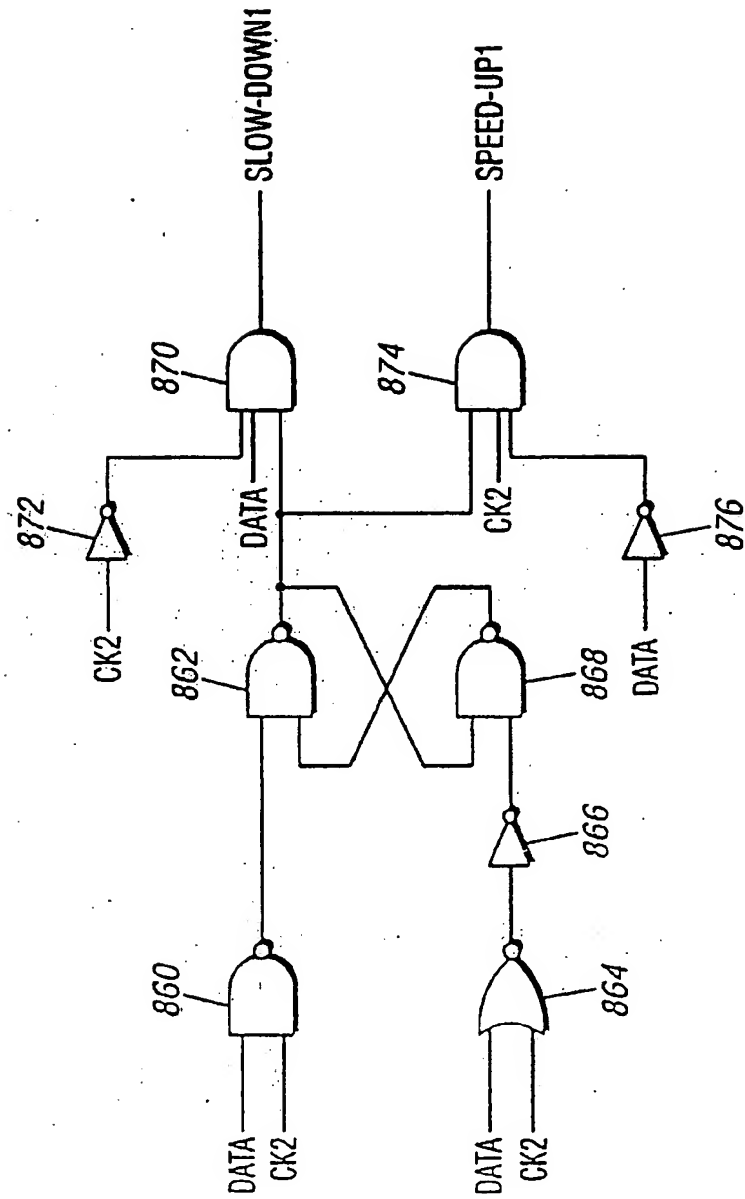


FIG. 9

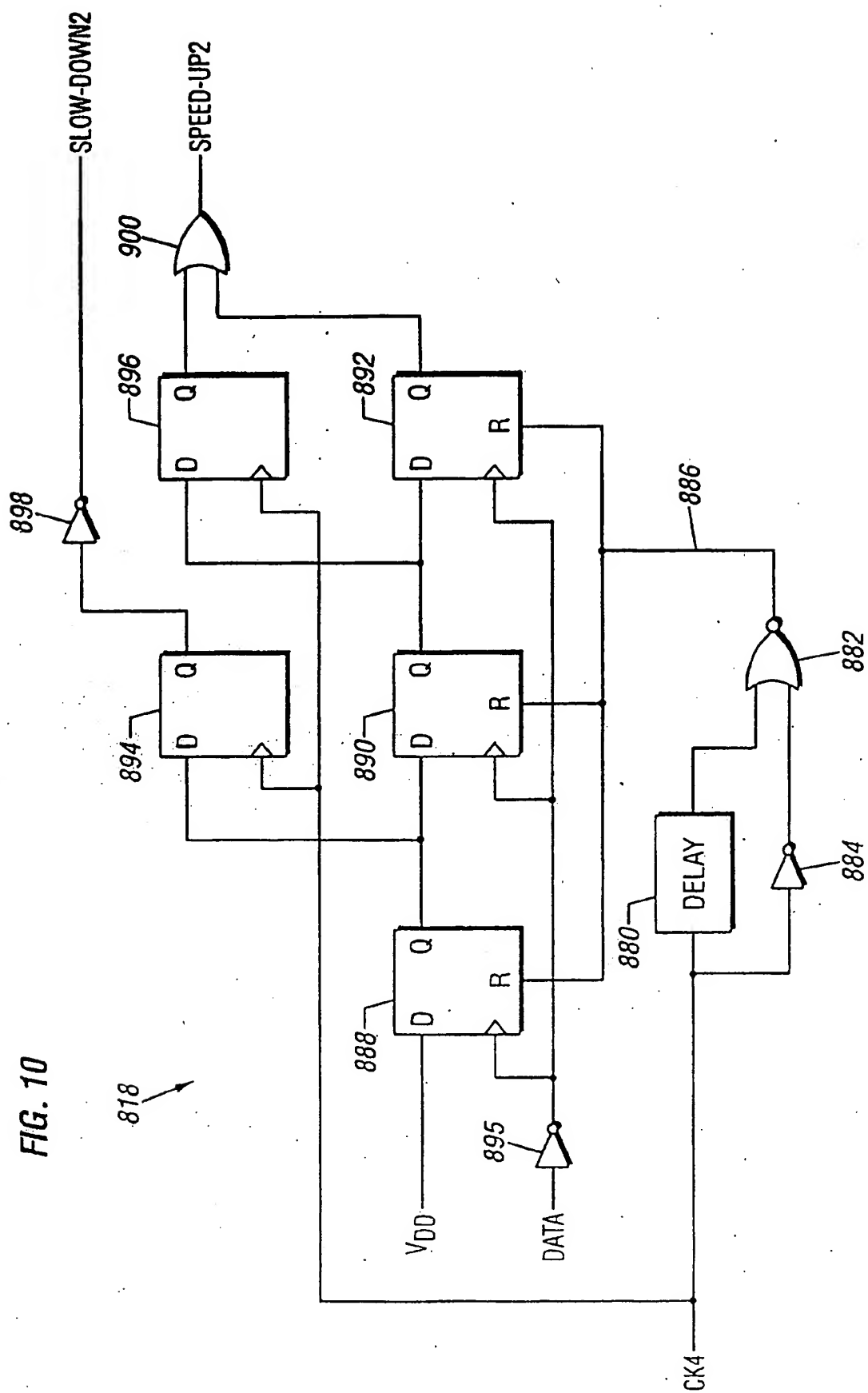


**FIG. 10**

818

The circuit diagram, labeled 818, shows a logic block with the following components and connections:

- Inputs:** CK4, DATA, and VDD.
- Flip-Flops:** Three D flip-flops (888, 890, 892) and two more D flip-flops (894, 896). Each has a clock input (triangle symbol), a D input, a Q output, and an R input.
- Logic Elements:**
  - Inverter 884: Input from CK4, output to the R input of flip-flop 888.
  - Inverter 895: Input from DATA, output to the R input of flip-flop 888.
  - Delay block 880: Input from CK4, output to the R input of flip-flop 890.
  - OR gate 882: Inputs from the Q outputs of flip-flops 888 and 890, output to the R input of flip-flop 892.
  - OR gate 900: Inputs from the Q outputs of flip-flops 894 and 896, output to the R input of flip-flop 892.
  - Inverter 898: Input from the Q output of flip-flop 894, output to the D input of flip-flop 896.
- Connections:**
  - CK4 is connected to the clock inputs of flip-flops 888, 890, and 892, and to the R input of flip-flop 888 via inverter 884.
  - DATA is connected to the R input of flip-flop 888 via inverter 895.
  - VDD is connected to the R inputs of flip-flops 888 and 890.
  - The Q output of flip-flop 888 is connected to the R input of flip-flop 890 via OR gate 882.
  - The Q output of flip-flop 890 is connected to the R input of flip-flop 892 via OR gate 882.
  - The Q output of flip-flop 892 is connected to the R input of flip-flop 894.
  - The Q output of flip-flop 894 is connected to the R input of flip-flop 896 via inverter 898.
  - The Q output of flip-flop 896 is connected to the R input of flip-flop 892 via OR gate 900.
- Outputs:** SLOW-DOWN2 (from the Q output of flip-flop 888) and SPEED-UP2 (from the Q output of flip-flop 892).



```

graph LR
    DataOut[DATA OUT 546] --> ShiftReg[SHIFT REGISTER 840]
    CK4[CK4] --> ShiftReg
    ShiftReg -- 842 --> FrameDetect[FRAME DETECT LOGIC 844]
    FrameDetect -- 848 --> MuxControl[MUX CONTROL LOGIC 830]
    Counter[COUNTER 850] --> MuxControl
    MuxControl -- MUX CONTROL --> DemuxLogic[DEMUX LOGIC 846]
    DemuxLogic -- DE-MUXED DATA --> Out[ ]
  
```

DATA	1	DATA	1	DATA	1	DATA	1	DATA	1	DATA	1	DATA	1	DATA	0	DATA	OFF HOOK
------	---	------	---	------	---	------	---	------	---	------	---	------	---	------	---	------	----------

860      862      864

FRAME

FIG. 13A

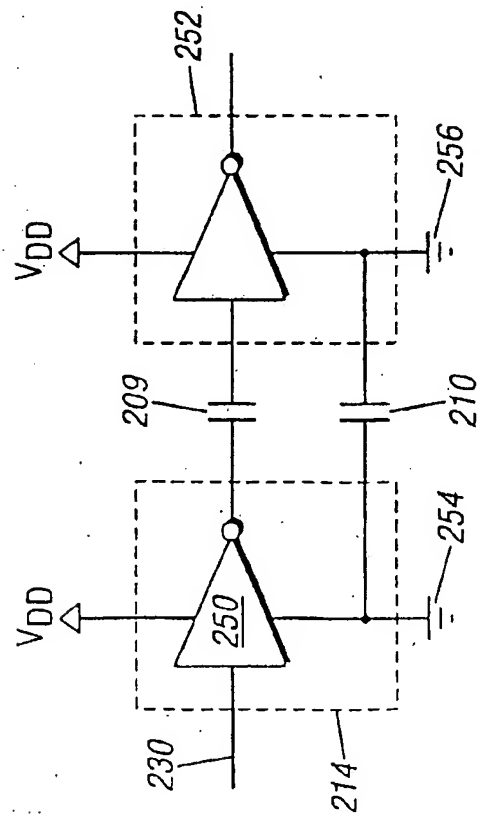


FIG. 13B

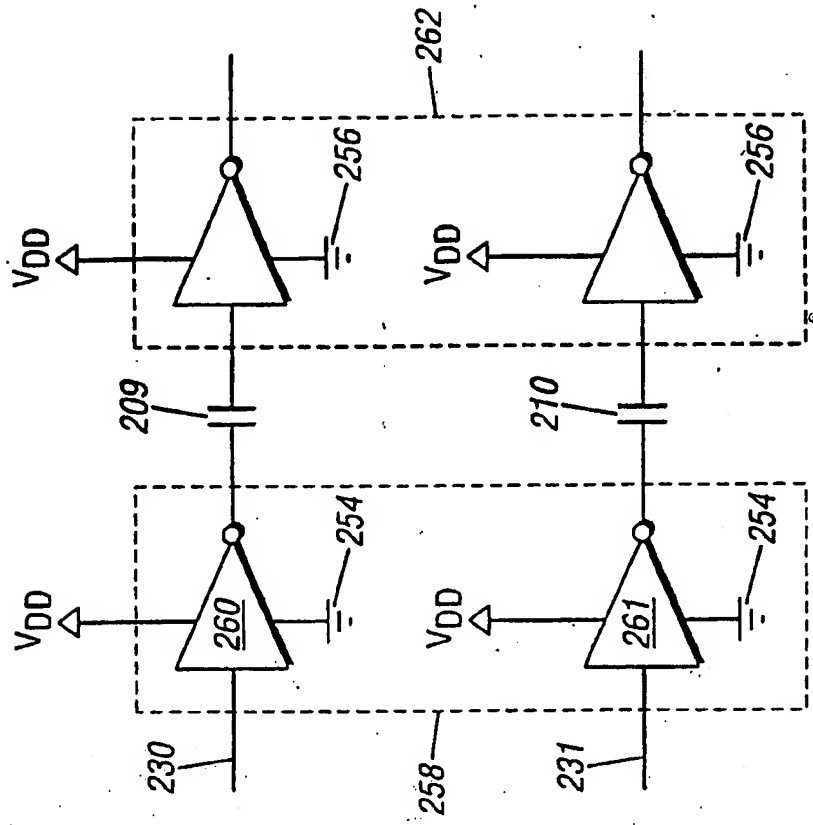


FIG. 14

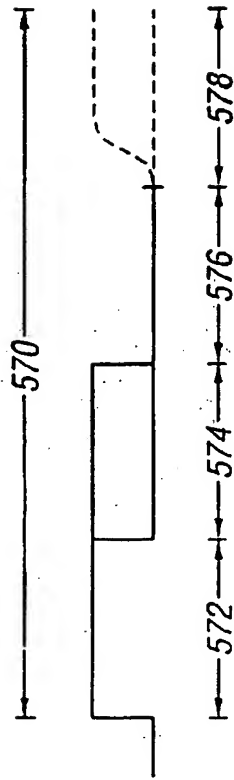
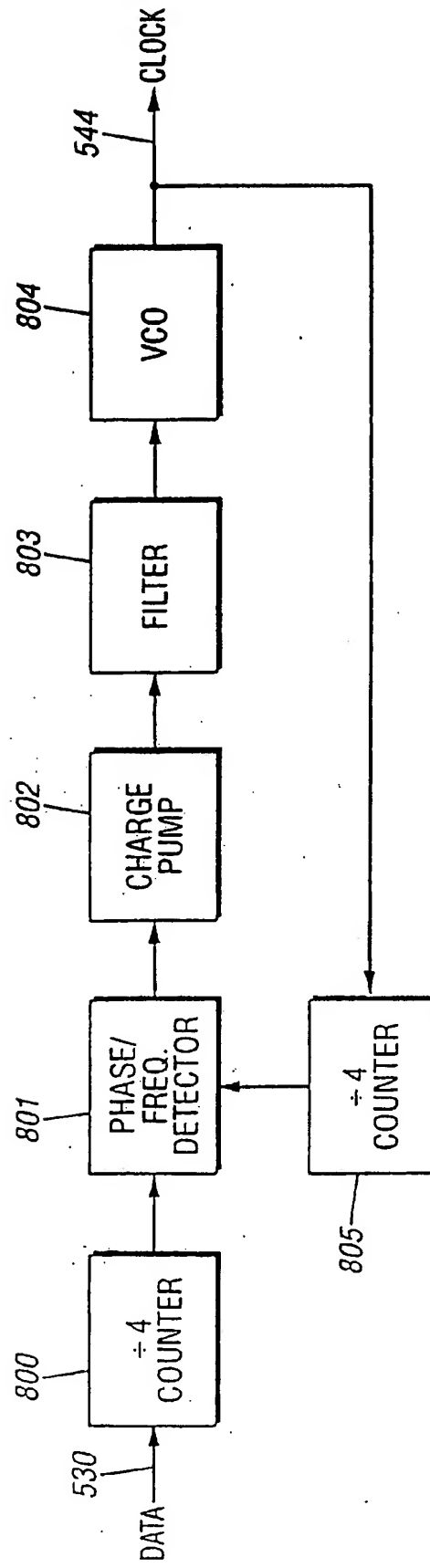


FIG. 15



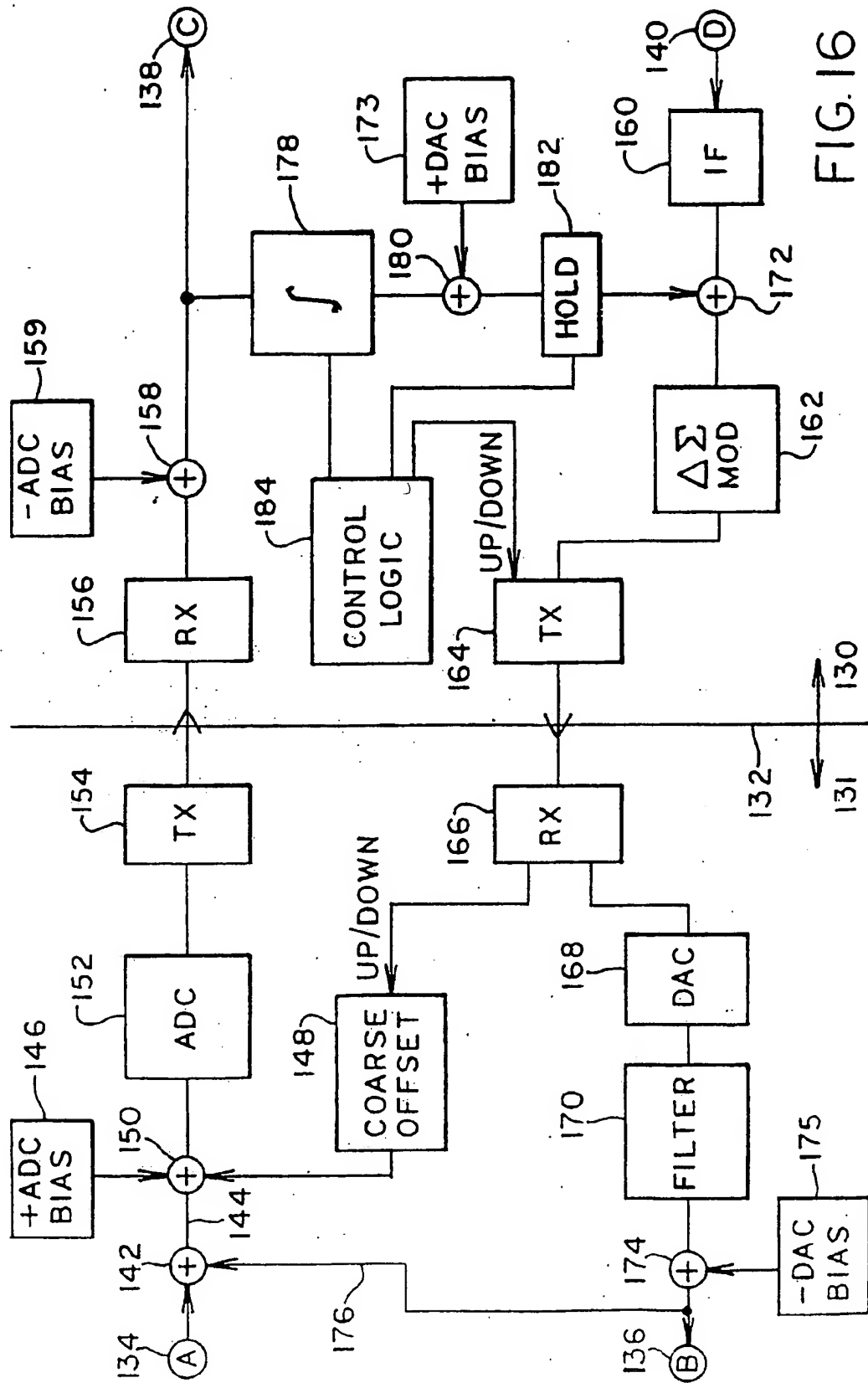


FIG. 16



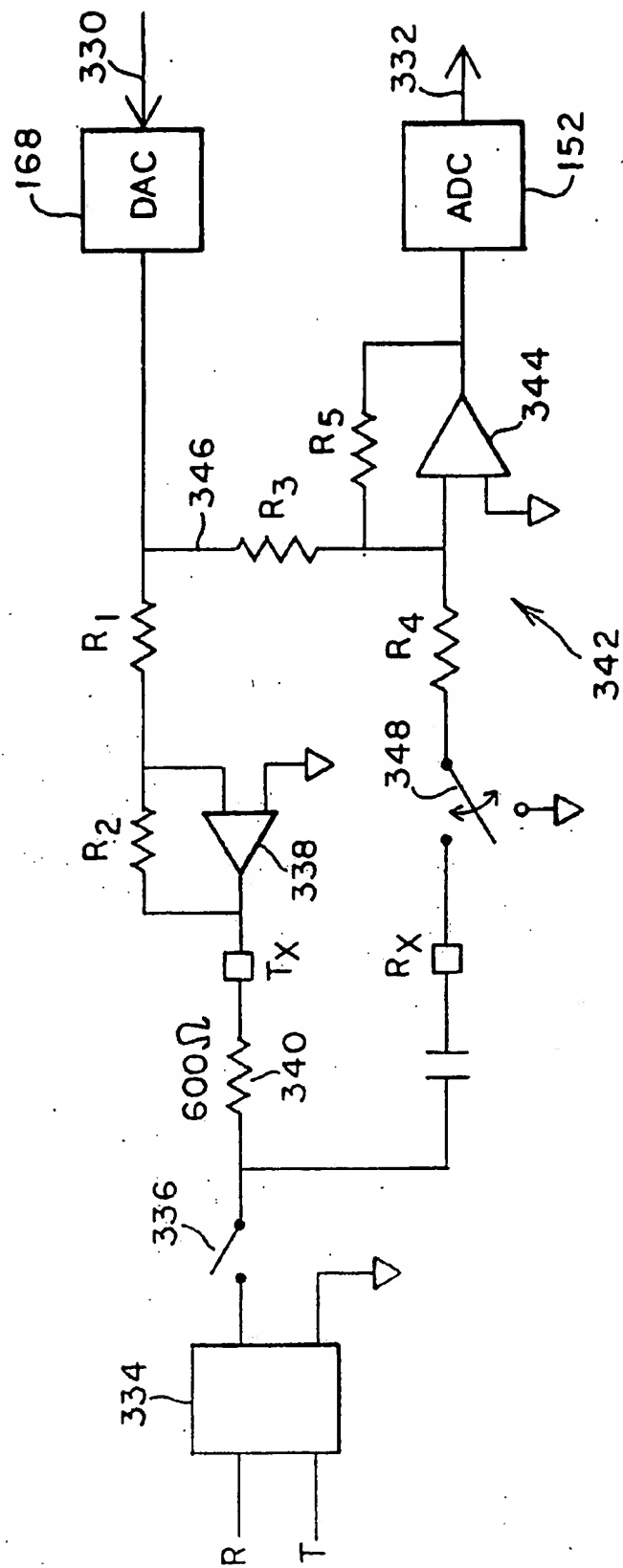


FIG. 17